

Letter

Tensor-Product Parity Code for Magnetic Recording

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In magnetic recording, a standard code architecture consists of an outer Reed–Solomon code in concatenation with an inner parity code. The inner parity code is used to detect and correct common error events. Generally, a parity code with short block length performs better, as multiple error events within one block and, consequently, miscorrection are less likely. In this paper, we study an inner code that offers the same system performance as a parity code with very short block length, even as short as the symbol length (in bits) of the outer Reed–Solomon code, but with higher code rate. This code is a tensor-product code, with a Bose–Chaudhuri–Hocquenghem (BCH) code and a short parity code as constituent codes. The decoder for this code is not much more complex than the optimal decoder of the baseline parity-coded channel; in fact, the only additional steps are Viterbi detection matched to the channel and decoding of the BCH code.

Index Terms—BCH code, magnetic recording, parity code, Reed–Solomon code, tensor-product code.

I. INTRODUCTION

AN error-control code is employed in magnetic recording to ensure data reliability. Reed–Solomon (RS) codes are, by far, the most commonly used for this purpose. To further improve the reliability, the RS code is often concatenated with an inner code that helps to correct random errors. Distance-enhancing codes and parity codes are well-known examples. In this paper, we will focus on schemes employing parity codes.

Despite performance benefits of short parity codes, their rate penalty is severe. Hence, high-rate parity codes with a block length on the order of 30 to 100 bits are often used. It is more likely that such a code will miscorrect, and hence propagate, errors. It is also more likely that multiple error events will occur within one block and therefore go undetected.

To overcome these deficiencies, we propose the use of a “tensor-product parity code” whose parity-check matrix is the tensor product [5] of the parity-check matrices of a short parity code and a BCH code. As we will show, this code has the same performance as a short parity code, but with higher rate.

II. SINGLE-PARITY CODES

The channel is assumed to have a Lorentzian step response with channel bit density $PW50 = 3$. The read signal is corrupted by additive white Gaussian noise (AWGN) with two-sided power spectral density σ^2 . The signal-to-noise ratio (SNR) is defined to be $10 \log_{10}(1/\sigma^2)$. The equalizer is a finite-impulse-response (FIR) filter with target polynomial $0.67 + 0.39D - 0.30D^2 - 0.49D^3 - 0.26D^4$.

Using a Viterbi detector matched to the target, we collected error events at SNR = 20 dB, corresponding to a bit error rate of 3.5×10^{-3} . Table I presents the number of error events of increasing length found in our simulation. The most common error events for this channel model are $+-+$ and $+$, which have odd Hamming weight. Thus, a single-parity-check code can detect isolated occurrences of these error events. This observation has

TABLE I

NUMBER OF ERROR EVENTS BASED ON LENGTH. A TOTAL OF 1000 SECTORS ARE SIMULATED FOR EACH CODING SCHEME. THE NUMBERS OF BITS PER SECTOR FOR UNCODED, RATE-30/31, AND RATE-10/11 PARITY CODES ARE 4680, 4692, AND 4686, RESPECTIVELY

error event length	uncoded	rate-30/31 single-parity	rate-10/11 single-parity
1	2828	0	0
2	951	1144	1090
3	2952	11	17
4	245	313	276
5	168	95	86
6	144	149	111
7	82	79	56
8	50	62	34
9	23	49	23
10	10	29	14
≥ 11	36	339	30

inspired several coding schemes that involve parity codes [1], [3].

An optimal sequence decoder for a parity-coded system is a Viterbi detector that combines channel states and code states [7]. Systems incorporating multiple-parity codes often use post-processing techniques to reduce decoder complexity while retaining near-optimal performance [7]. The systems considered in this paper, however, incorporate only single-parity codes, so optimal decoders are used in simulations.

Table I shows the number of error events of increasing length in parity-coded channels using single-parity codes of rate 30/31 and 10/11. We see that, in comparison to the uncoded case, the rate-30/31 parity-coded channel has many more error events of length 8 or higher, whereas, when the rate-10/11 code is used, there are fewer error events than in the uncoded system at almost all event lengths. This translates into a larger sector error rate for the higher rate system.

III. TENSOR-PRODUCT PARITY CODE SYSTEM

The results in the previous section show that shorter parity codes can improve performance at the cost of a reduced code rate. In this section, we study a modified parity-coding scheme that, with less redundancy, achieves the performance of a short parity code.

A. Code Construction

Let C_1 be an (n_1, k_1) parity code and let C_2 be an (n_2, k_2) binary linear code such that $n_1 - k_1$ divides n_2 . We consider the code C with the following properties.

- C is an (n, k) binary linear code such that $n = k_1 n_2 / (n_1 - k_1)$ and $k = n - n_2 + k_2$.
- Suppose we divide a codeword of C into disjoint blocks of length k_1 , and compute the parity bits for each block using C_1 . The parity bits of all blocks must form a valid codeword of C_2 .

We construct a parity-check matrix for the code C , as follows. We assume that the parity-check matrix of C_1 has the form $H_1 = [H'_1 \ I]$, where H'_1 is an $(n_1 - k_1) \times k_1$ matrix and I is the identity matrix of size $n_1 - k_1$. Let \mathbf{v}_m denote the m th row of H'_1 . Now, let $H_2 = [h_{i,j}]$ be a parity-check matrix of C_2 , and define H to be the matrix whose l th row is given by the vector in (1), shown at the bottom of the page. It can be shown that the code C defined by the parity-check matrix H has the properties specified above.

When C_1 is a single-parity code, the code C is a special case of a tensor-product code [5] and an error-location code [6], [4]. In the general case, the code C can be viewed as a generalized tensor-product code [2]. We therefore refer to C as a *tensor-product parity code*. The message length k_1 of C_1 is called the *block size* of C .

The tensor-product parity code can be concatenated with an RS outer code, but we will, instead, combine the codes by taking their common subspace. More precisely, let C_3 be an (n_3, k_3) RS code over $\text{GF}(2^q)$ such that $qn_3 = n$, the codeword length of the tensor-product parity code. Let H_3 be a binary parity-check matrix of C_3 . (Thus, H_3 is a $q(n_3 - k_3) \times qn_3$ matrix.) Then the combined code C' is defined by the following parity-check matrix:

$$H' = \begin{bmatrix} H_3 \\ H \end{bmatrix}. \quad (2)$$

In a slight abuse of terminology, we will call C_2 the *inner code* and C_3 the *outer code*.

B. An Example

Let C_1 be the $(n_1, k_1) = (4, 3)$ single-parity code. The parity-check matrix for C_1 is $H_1 = [1 \ 1 \ 1 \ 1]$. Let C_2 be the $(7, 4)$ Hamming code. A parity-check matrix for C_2 is

$$H_2 = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 & 1 \end{bmatrix}.$$

The parity-check matrix of the tensor-product parity code is

$$H = \begin{bmatrix} 111 & 000 & 000 & 000 & 111 & 111 & 111 \\ 000 & 111 & 000 & 111 & 000 & 111 & 111 \\ 000 & 000 & 111 & 111 & 111 & 000 & 111 \end{bmatrix}.$$

TABLE II

POSSIBLE CHOICES OF BCH CODES AND RS CODES WITH TOTAL REDUNDANCY OF APPROXIMATELY 580 BITS

t_{RS}	RS redundancy	t_{BCH}	BCH redundancy	total redundancy
14	280	41	300	580
15	300	38	282	582
16	320	31	261	581
17	340	29	243	583
18	360	26	216	576
19	380	23	198	578
20	400	21	180	580

Let C_3 be a binary form of the $(7, 5)$ RS code over $\text{GF}(8)$. Then C_3 is a $(21, 15)$ binary code. The parity-check matrix H' of the combined code is computed by appending H to a parity-check matrix of C_3 as in (2). The combined code can be made systematic by applying suitable row operations to H' .

C. Encoding

For simplicity, we assume that C_1 is a single-parity code. The following encoding method can be easily extended to the general case. First, observe that if H_2 is in the systematic form as in the above example, columns $k_1, 2k_1, \dots, (n_2 - k_2)k_1$ of H form the identity matrix. Thus, we can use H directly to compute the redundancy bits and insert them at the corresponding positions. To be more efficient, take $k_2 k_1$ information bits and divide them into k_2 blocks. Compute the parity of each block and encode the parity using C_2 . Take the rest of the information bits $((n_2 - k_2)(k_1 - 1))$ bits and divide them into $n_2 - k_2$ blocks. Compute the parity of each block. The redundancy bits of the tensor-product parity code are the modulo-2 sum of these parity bits and the parity part of C_2 .

D. Decoding

Decoding of the tensor-product parity-coded system begins with detection of the recorded bits using the Viterbi algorithm matched to the channel only. Then, the parity bits are computed using the encoder for C_1 , and the resulting word is decoded using the decoder for C_2 . The corrected parity bits are provided to a Viterbi detector reflecting channel states and parity code states, and the detector output sequence is decoded by the outer decoder.

IV. PERFORMANCE COMPARISON

Consider the $(468, 410)$ RS code over $\text{GF}(1024)$. This code has 580-bit redundancy and can correct 29 symbol errors. To construct a tensor-product parity code with a similar code rate, we choose the codes C_1, C_2, C_3 as follows.

Fix C_1 to be the $(11, 10)$ single-parity code; that is, the block size is 10. Let C_3 be a $(468, k_3)$ RS code with error-correcting capability $t_{\text{RS}} = (468 - k_3)/2$. Choose C_2 to be a $(468, k_2)$ binary BCH code such that the total redundancy $10(468 - k_3) + 468 - k_2$ is close to 580 bits. Denote the error-correcting capability of the BCH code by t_{BCH} . Table II shows some possible combinations of C_2 and C_3 that have comparable redundancy.

$$\left[\sum_{m=1}^{n_1-k_1} h_{\ell, m} \mathbf{v}_m \quad \sum_{m=1}^{n_1-k_1} h_{\ell, n_1-k_1+m} \mathbf{v}_m \quad \cdots \quad \sum_{m=1}^{n_1-k_1} h_{\ell, ((n_2/(n_1-k_1))-1)(n_1-k_1)+m} \mathbf{v}_m \right]. \quad (1)$$

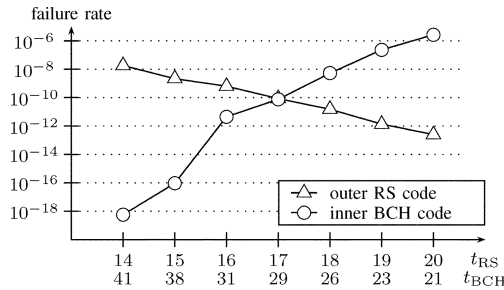


Fig. 1. Failure rates at SNR = 20 dB of the outer RS code and the inner BCH code as a function of their error-correcting capabilities (t_{RS} and t_{BCH}). The block size is fixed to be 10.

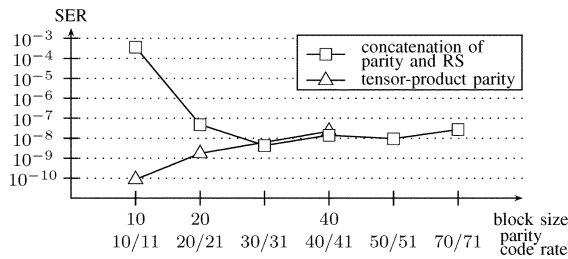


Fig. 2. Analytic sector error rates at SNR = 20 dB of the tensor-product parity code scheme and the concatenation of a parity code with an RS code. The block size of the tensor-product parity code is varied from 10 to 40. For the concatenation scheme, the rate of the parity code is varied from 10/11 to 70/71.

To choose the best combination, we fix the SNR at 20 dB and estimate the sector error rate (SER) of each combination by an analytical method based on a block multinomial model [3]. The failure rates for inner code and outer code are plotted in Fig. 1. The SER of the combined code is approximately the maximum of these two failure rates. The figure indicates that the 17-error-correcting RS code and the 29-error-correcting BCH code are the best combination at this SNR. The combined code is a (4680, 4097) code.

Next, we vary the block size k_1 and estimate the SER. The result is plotted in Fig. 2. Also shown is the SER of the concatenation of a parity code and an RS code, whose total redundancy is approximately 580 bits. For the concatenation scheme, a high-rate parity code is preferred since a low-rate parity code only allows a weak RS code. In contrast, the tensor-product parity code scheme gives lower SER when it has a smaller block size. When the block size is large, the SER is comparable to the concatenation scheme since the best inner code C_2 is the trivial code with one codeword. (When C_2 has only the zero codeword, the tensor-product parity code becomes a single-parity code.)

Finally, we select the best parameters for the concatenation scheme and the tensor-product parity code scheme and compare their performance to that of the (468, 410) RS code. Analytic results and computer simulation results are shown in Figs. 3 and 4, respectively. We see that the tensor-product parity code scheme has a gain of approximately 0.3 dB over the RS code and almost 0.2 dB over the concatenation scheme at SER = 10^{-10} . In general, the slope of the failure rate of a code is steeper if the code is stronger. Thus, the SER of the RS code falls more rapidly than that of the concatenation scheme; they eventually cross near SNR = 21 dB. For SNR < 20 dB, the SER of the tensor-product parity code scheme is dominated by the failure rate of the inner code. Hence, in this region, the SER slope is

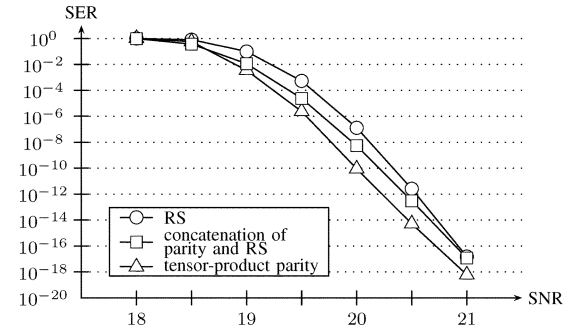


Fig. 3. Analytic sector error rates of the (468, 410) RS code, the concatenation of the rate-30/31 parity code and the (454, 410) RS code, and the tensor-product parity code scheme with block size 10, (468, 225) inner BCH code, and (468, 434) outer RS code.

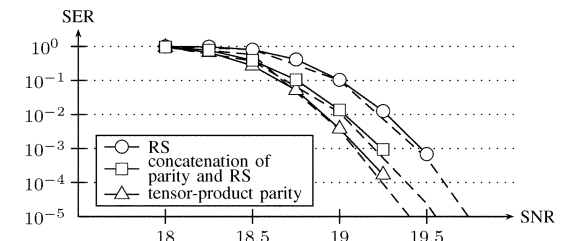


Fig. 4. Simulated sector error rates of the three codes described in Fig. 3. The dashed lines are the analytic sector error rates shown in Fig. 3.

comparable to that of the RS-only scheme. For SNR > 20 dB, the failure rate of the outer code becomes dominant and the slope changes substantially. (The reason that this change occurs near SNR = 20 dB is that we choose the inner and outer codes based on the SER at SNR = 20 dB.) Although not shown here, the SER performance obtained using double-parity codes showed no additional improvement.

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